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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,431	11/28/2003	Takayuki Kondo	117603	7372

25944 7590 12/08/2006

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EXAMINER	
PEACE, RHONDA S	

ART UNIT	PAPER NUMBER
2874	

DATE MAILED: 12/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/722,431	KONDO, TAKAYUKI	
	Examiner	Art Unit	
	Rhonda S. Peace	2874	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-6,8,9,12-16 and 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3,4,6,8,9,12-16 and 24* is/are rejected.

7)☒ Claim(s) *2 and 5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/31/06, 10/5/06, 11/16/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/25/2006 has been entered.

Information Disclosure Statement

The information disclosure statements (IDS) submitted on 8/31/2006, 10/5/2006, and 11/16/2006 were filed in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 3, 4, 6, 8, 12-16, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Worley (US 6393183).

Pertaining to claim 16, Worley discloses an optical interconnection circuit comprising (see col. 4 lines 64-67, col. 5 lines1-6, Fig 1):

- An integrated circuit as seen in Figure 1.

- A first circuit block **102** provided on the integrated circuit chip of Figure 1, where the first block **102** contains a first element **101** for emitting light.
- A second circuit block **105** provided on the integrated circuit chip of Figure 1, where the second block **105** contains a second element **103** for receiving light.
- An optical waveguide **100A**, provided on the circuit chip such that the waveguide **100A** optically connects the first element **101** to the second element **103**.

Further pertaining to claim 16, the embodiment of Worley discussed above involves the use of vertical emitting laser diodes. However, the above device may be modified as seen in Figure 2G such that a side emitting laser diode is utilized. In this embodiment using a side emitting laser diode **212**, a reflector **214** is used to redirect any vertical-emitted light into the waveguide **209** (col. 7 lines 37-67, Fig 2G). Moreover, Worley discloses the blocks **102** and **105** (or any such blocks described therein, such as **202**, **205**, etc) may contain a plurality of light emitters, such as light emitter **101**, or a plurality of light detectors, such as detector **103**, respectively, where each emitter/detector pair (one on each block) will communicate via an optically isolated channel (col. 9 lines 52-58). In view of this teaching of Worley, it would have been obvious to one of ordinary skill in the art to allow block **102** to contain a plurality of light emitters, and also allow block **105** contain a plurality of light detectors, where each emitter/detector pair will be connected via their own waveguide such as waveguide **100A**, as the use of a greater number of emitter/detector pairs allows a greater amount

of information to be transferred between the two blocks **102** and **105**. In the event multiple emitters **212** are utilized on the same block **202**, as discussed above, numerous reflectors **214** would be used for each emitter **212**; however, it would be obvious to one of ordinary skill in the art to use an elongated bar-shaped reflector (instead of several square shaped reflectors), as using a single reflector reduces production time of the device, as the coupling process between the emitters and reflector (as opposed to emitters and reflectors) requires less precision, and therefore, less time.

In conclusion with respect to claim 16, Worley also discloses the light emitter **101** produces visible light, but does not disclose that when a plurality of light emitters are placed upon the first block **102** each emitter emits a unique wavelength (col. 5 lines 6-13). However, in view of the teaching that the emitter emits visible light, which is well-known to contain a plurality of unique wavelengths, it would have been obvious to one of ordinary skill in the art to allow the plurality of emitters on the first block to each emit a unique wavelength. In addition to this suggestion made by Worley, the use of multiple wavelengths for transmission purposes has other advantages, such as allowing for versatility when processing such signals, as signals of multiple wavelengths can then be processed by various methods and devices.

Concerning claims 3 and 4, Worley shows in Figure 2G that a portion of the waveguide **209** is provided on the top surface of the circuit blocks **202** and **205**, specifically upon the top surface of trenches **210** and **211** respectively (col. 7 lines 52-60). It is of special note that the top surface of trenches **210** and **211** is considered a

portion of the top surface of each block **202** and **205**, as this surface is the upper most surface of the block in the area of the trenches **210** and **211**. As also seen in Figure 2G, the waveguide **209** transverses the first and second blocks **202** and **205**.

With regard to claims 6, 8, Worley discloses the light emitters **101** of block **102**, and the light detectors **103** of block **105** are each electrically connected to their respective block (col. 8 lines 41-44). Moreover, Figure 2G shows an additional embodiment, where the outer edge of waveguide **218** acts as a reflector in the region directly above each of the emitter **201** and detector **203**, such that light is coupled through the waveguide **218** from the emitter **201** to the detector **203** (col. 7 lines 38-40). As seen in Figure 2G, a portion of the waveguide **218** extends over the emitter **212**, and a portion extends over the detector **216** (col. 7 lines 19-22).

Pertaining to claims 12 and 13, Worley discloses the above described connection method as being useful in optically joining two electrically separate integrated circuits (col. 1 lines 20-25). In the case where several devices or integrated circuits, as described above, are adjacent one another, one of ordinary skill in the art would have been motivated to join the two or more integrated circuits in the same manner as described above, as Worley discloses such a coupling method (coupling an emitter of one circuit to a detector of another circuit via an optical waveguide) can improve the light coupling efficiency from an LED to a detector over that of the prior art, such as a simple transparent insulating block (col. 3 lines 29-33). Moreover, it would have been obvious to one of ordinary skill in the art to combine several adjacent integrated circuit chips together onto a single substrate, as this improve stability of the device, thereby

leading to a reliable coupling between the chips upon the substrate. Finally, it would have been obvious to one of ordinary skill in the art to bond the chips tightly to one another, as this will further decrease the overall size of the device making it more applicable to compact applications, as well as further ensuring a sound optical connection between the chips via the coupling method described above.

Concerning claims 14 and 15, the device of Worley described above may be considered both an electronic and an electro-optical device, as the device converts electrical signals to optical signals and visa versa.

Pertaining to claim 24, the reflector **214**, as explained above, allows the light emitted from emitter **212** to be coupled into the waveguide **209** (Fig 2G).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Worley (US 6393183) in further view of Ewen et al (US 6735731).

Concerning claim 9, Worley discloses the device as described above. However, Worley does not disclose either of the blocks as being one of the following: CPU, memory circuit, DSP, RF amplifying circuit, image sensor, and bio sensor. Moreover, Worley does not disclose the waveguides as transmitting data or clock signals.

Further concerning claim 9, Ewen et al discloses parallel transceivers **110** and **120**, optically connected via optical transmission lines, where there is provided a single line for each channel (Fig 1, col. 2 lines 58-67, col. 3 lines 1-21). Transceiver **110** is a memory circuit with memory circuitry **114**; transceiver **120** is an image sensor, with image (light) error detection circuitry **124** (col. 4 lines 10-24, col. 5 lines 22-24).

Moreover, at least one optical waveguide connecting the first transceiver **110** to the second transceiver **120** transmit clock signals (col. 3 lines 39-50). It would have been obvious to one of ordinary skill to incorporate the coupling teachings of Worley to the device of Ewen et al, as Worley discloses such a coupling method can improve the light coupling efficiency from an LED to a detector over that of the prior art (col. 3 lines 29-33).

Allowable Subject Matter

Claims 2 and 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The applicable prior art does not disclose, nor does it reasonably suggest, an optical interconnection unit as described in claim 16, and further providing either of the following: the first and second blocks are electrically connected to each other, or a part of the first waveguide being provided to detour around a third circuit block. Worley, considered to be the closest piece of art to independent claim 16, is concerned with optically coupling two blocks that must remain electrically isolated from one another. Therefore, there is no disclosure or motivation to electrically connect the blocks. In addition, in all embodiments of Worley, the waveguides are either routed on the top surface of the blocks, suspended over the blocks, or travels through the blocks. Therefore, there is no teaching or motivation to suggest routing a waveguide around a third block.

Response to Arguments

Applicant's arguments, see page 6, filed 10/25/2006, with respect to the objections of claims 8 and 13 have been fully considered and are persuasive. The objections of claims 8 and 13 have been withdrawn.

Applicant's arguments, see pages 6-8, filed 10/25/2006, with respect to the rejection(s) of claim(s) 2-6, 8, 9, and 12-23 under 35 U.S.C. §103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made primarily in view of Worley, as discussed at length above.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kondo (US 2004/0264867, US 2004/0136639, 2004/0131304) discloses an optical interconnection circuit. Janniello et al (US 5537238) discloses a WDM system. Bregman et al (US 5093879) discloses an electro-optical connector. Asai (US 2005/0185880) discloses an integrated circuit and device for optical communication. Pan (US 6038357) discloses PDM-WDM for optical communication networks. Jain et al (US 2005/0111781) discloses a photonic-electronic circuit board. Shen et al (US 2004/0218848) discloses a flexible electro-optical interconnection film. Ouchi (US 2004/0081402) discloses an optical interconnection device. Kuhara et al (US 2003/0152391) discloses a parallel line emitting and receiving device. Jewell et al (US 2001/0021287) discloses an electro-optical mechanical assembly for coupling a light source to a detector. Bi et al (US 6952504) discloses the three-dimensional

engineering structures of optical structures. Takai et al (US 5448661) discloses an optical parallel transmission device. Mayer et al (US 6816642) discloses the use of optical fiber arrays in communication systems.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rhonda S. Peace whose telephone number is (571) 272-8580. The examiner can normally be reached on M-F (8-5).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rodney Bovernick can be reached on (571) 272- 2344. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Rhonda S. Peace
Examiner
Art Unit 2874

John D. Lee
Primary Examiner